查询SST29EE010-120-3C-E供应商

1 Megabit (128K x 8) Page Mode EEPROM
SST29EE010, SST29LE010, SST29VE010

Data Sheet

FEATURES:

- **Single Voltage Read and Write Operations**
  - 5.0V-only for the 29EE010
  - 3.0V-only for the 29LE010
  - 2.7V-only for the 29VE010
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 20 mA (typical) for 5V and 10 mA (typical) for 3.0/2.7V
  - Standby Current: 10 µA (typical)
- **Fast Page-Write Operation**
  - 128 Bytes per Page, 1024 Pages
  - Page-Write Cycle: 5 ms (typical)
  - Complete Memory Rewrite: 5 sec (typical)
  - Effective Byte-write Cycle Time: 39 µs (typical)
- **Fast Read Access Time**
  - 5.0V-only operation: 90 and 120 ns
  - 3.0V-only operation: 150 and 200 ns
  - 2.7V-only operation: 200 and 250 ns
- **Latched Address and Data**
- **Automatic Write Timing**
  - Internal V_{pp} Generation
- **End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **Hardware and Software Data Protection**
- **TTL I/O Compatibility**
- **JEDEC Standard Byte-wide EEPROM Pinouts**
- **Packages Available**
  - 32-Pin TSOP (8x20 & 8x14 mm)
  - 32-Lead PLCC
  - 32 Pin Plastic DIP

PRODUCT DESCRIPTION

The 29EE010/29LE010/29VE010 are 128K x 8 CMOS page mode EEPROMs manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29EE010/29LE010/29VE010 write with a single power supply. Internal Erase/Program is transparent to the user. The 29EE010/29LE010/29VE010 conform to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29EE010/29LE010/29VE010 provide a typical byte-write time of 39 µsec. The entire memory, i.e., 128K bytes, can be written page by page in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29EE010/29LE010/29VE010 have on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29EE010/29LE010/29VE010 are offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29EE010/29LE010/29VE010 are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29EE010/29LE010/29VE010 significantly improve performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29EE010/29LE010/29VE010 improve flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29EE010/29LE010/29VE010 are offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 1 and 2 for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29EE010/29LE010/29VE010 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29EE010/29LE010/29VE010 have industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29EE010/29LE010/29VE010 are compatible with industry standard EEPROM pinouts and functionality.

Read

The Read operations of the 29EE010/29LE010/29VE010 are controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the

© 1998 Silicon Storage Technology, Inc. The SST logo and SuperFlash are registered trademarks of Silicon Storage Technology, Inc. These specifications are subject to change without notice.

chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The Page Write to the SST29EE010/29LE010/29VE010 should always use the JEDEC Standard Software Data Protection (SDP) 3-byte command sequence. The 29EE010/29LE010/29VE010 contain the optional JEDEC approved Software Data Protection scheme. SST recommends that SDP always be enabled, thus, the description of the Write operations will be given using the SDP enabled format**. The 3-byte SDP Enable and SDP Write commands are identical; therefore, any time a SDP Write command is issued, software data protection is automatically assured.** The first time the 3-byte SDP command is given, the device becomes SDP enabled. Subsequent issuance of the same command bypasses the data protection for the page being written. At the end of the desired page write, the entire device remains protected. For additional descriptions, please see the application notes on "The Proper Use of JEDEC Standard Software Data Protection" and "Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories" in this data book.

The Write operation consists of three steps. Step 1 is the three byte load sequence for Software Data Protection. Step 2 is the byte-load cycle to a page buffer of the 29EE010/29LE010/29VE010. Steps 1 and 2 use the same timing for both operations. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During both the SDP 3-byte load sequence and the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by the T_{BLCO} timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 14 and 16 for flowcharts.

The Write operation has three functional cycles: the Software Data Protection load sequence, the page load cycle, and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that allows writing to the selected page and will leave the 29EE010/29LE010/29VE010 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the Write operation, the only valid reads are Data# Polling and Toggle Bit.

The Page-Write operation allows the loading of up to 128 bytes of data into the page buffer of the 29EE010/29LE010/29VE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29EE010/29LE010/29VE010 allow the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each Page-Write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e. A_7 through A_{16}. Any byte not loaded with user data will be written to FF.

See Figures 4 and 5 for the page-write cycle timing diagrams. If after the completion of the 3-byte SDP load sequence or the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29EE010/29LE010/29VE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29EE010/29LE010/29VE010 provide a Chip-Erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 9 for timing diagram, and Figure 18 for the flowchart.

© 1998 Silicon Storage Technology, Inc.

Write Operation Status Detection

The 29EE010/29LE010/29VE010 provide two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29EE010/29LE010/29VE010 are in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 15 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e. toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 15 for a flowchart. The initial read of the Toggle Bit will typically be a "1".

Data Protection

The 29EE010/29LE010/29VE010 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29EE010/29LE010/29VE010 provide the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., Write and Chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29EE010/29LE010/29VE010 are shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figures 4 and 5). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figures 4 and 5 for the timing diagrams. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 8 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 16 for flowcharts.

The 29EE010/29LE010/29VE010 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

© 1998 Silicon Storage Technology, Inc.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29EE010/29LE010/29VE010 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Please refer to the following Application Notes located at the back of this databook for more information on using SDP:

- Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories
- The Proper Use of JEDEC Standard Software Data Protection

Product Identification

The product identification mode identifies the device as the 29EE010/29LE010/29VE010 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29EE010/29LE010/29VE010. Users may wish to use the software product identification operation to identify the part (i.e. using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the software ID entry and read timing diagram and Figure 17 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

TABLE 1: PRODUCT IDENTIFICATION TABLE

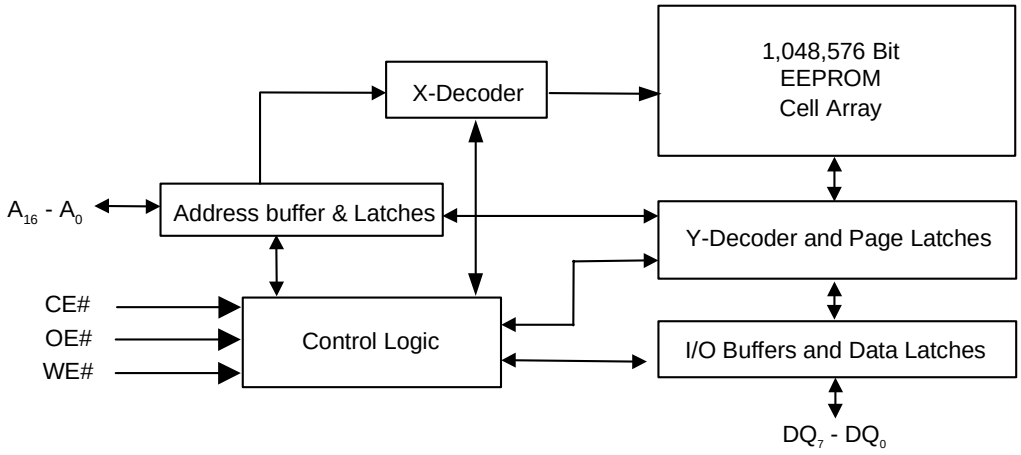
	Byte	Data
Manufacturer's Code	0000 H	BF H
29EE010 Device Code	0001 H	07 H
29LE010 Device Code	0001 H	08 H
29VE010 Device Code	0001 H	08 H

304 PGM T1.1

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The Reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g. not read correctly. See Table 4 for software command codes, Figure 11 for timing waveform and Figure 17 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM OF SST 29EE010/29LE010/29VE010



304 MSW B1.0

© 1998 Silicon Storage Technology, Inc.

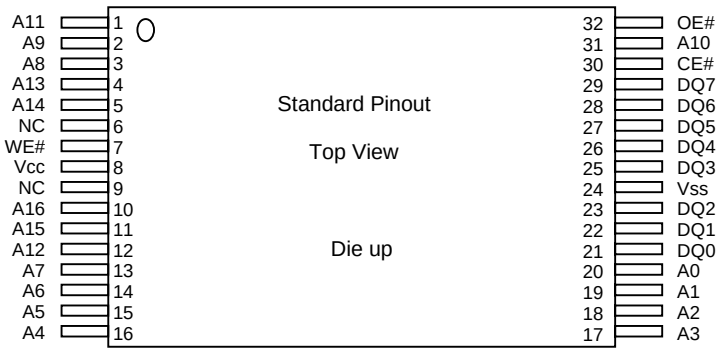


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGES

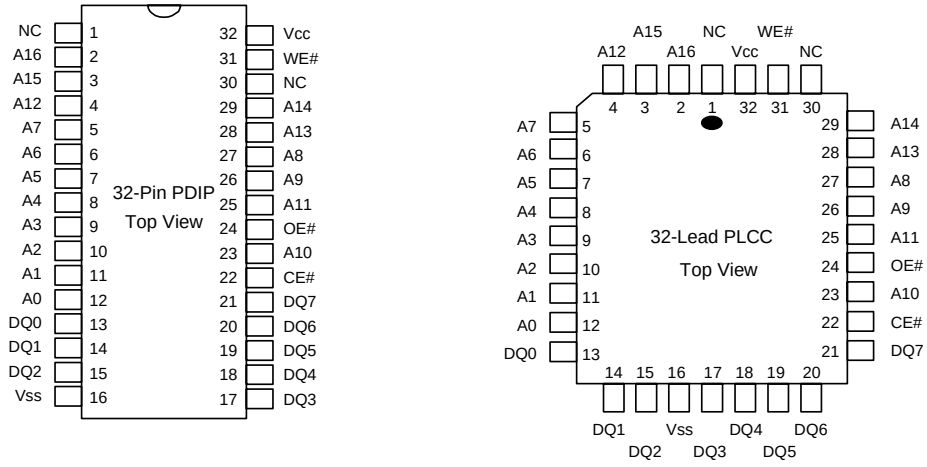


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLASTIC DIPS AND 32-LEAD PLCCS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{16}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 5-volt supply (± 10%) for the 29EE010, 3-volt supply (3.0-3.6V) for the 29LE010 and 2.7-volt supply (2.7-3.6V) for the 29VE010
Vss	Ground	
NC	No Connection	Unconnected pins.

304 PGM T2.0

© 1998 Silicon Storage Technology, Inc.

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (see notes)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

304 PGM T3.0

TABLE 4: SOFTWARE COMMAND CODES

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr(2)	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry(3)	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

304 PGM T4.1

Notes: (1) Address format A_{14}-A_0 (Hex), Addresses A_{15} and A_{16} are a "Don't Care".
(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).
(3) Alternate 6 byte software Product-ID Command Code
(4) The software chip erase function is not supported by the industrial temperature part.
Please contact SST, if you require this function for an industrial temperature part.

Notes for Software Product ID Command Code:
1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
29EE010 Device Code = 07H, is read with A_0 = 1.
29LE010/29VE010 Device Code = 08H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

© 1998 Silicon Storage Technology, Inc.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

29EE010 OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	5V±10%
Industrial	-40°C to +85°C	5V±10%

29LE010 OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	3.0V to 3.6V
Industrial	-40°C to +85°C	3.0V to 3.6V

29VE010 OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... 1 TTL Gate and C_L = 100 pF
See Figures 12 and 13

© 1998 Silicon Storage Technology, Inc.

TABLE 5: 29EE010 DC OPERATING CHARACTERISTICS V_{CC} = 5V±10%

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open,
	Read		30	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE#=OE#=WE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

304 PGM T5.0

TABLE 6: 29LE010/29VE010 DC OPERATING CHARACTERISTICS V_{CC} = 3.0-3.6 FOR 29LE010, V_{CC} = 2.7-3.6 FOR 29VE010

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

304 PGM T6.0

© 1998 Silicon Storage Technology, Inc.

TABLE 7: POWER-UP TIMINGS

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Write Operation	5	ms

304 PGM T7.0

TABLE 8: CAPACITANCE (T_a = 25 °C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

304 PGM T8.0

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	10,000(2)	Cycles	MIL-STD-883, Method 1033
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100	mA	JEDEC Standard 78

304 PGM T9.1

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
(2)See Ordering Information for desired type.

© 1998 Silicon Storage Technology, Inc.

AC CHARACTERISTICS

TABLE 10: 29EE010 READ CYCLE TIMING PARAMETERS

Symbol	Parameter	29EE010-90		29EE010-120		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	90		120		ns
T_{CE}	Chip Enable Access Time		90		120	ns
T_{AA}	Address Access Time		90		120	ns
T_{OE}	Output Enable Access Time		40		50	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		30		30	ns
T_{OHZ}(1)	OE# High to High-Z Output		30		30	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

304 PGM T10.1

TABLE 11: 29LE010 READ CYCLE TIMING PARAMETERS

Symbol	Parameter	29LE010-150		29LE010-200		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	150		200		ns
T_{CE}	Chip Enable Access Time		150		200	ns
T_{AA}	Address Access Time		150		200	ns
T_{OE}	Output Enable Access Time		60		100	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		30		50	ns
T_{OHZ}(1)	OE# High to High-Z Output		30		50	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

304 PGM T11.0

TABLE 12: 29VE010 READ CYCLE TIMING PARAMETERS

Symbol	Parameter	29VE010-200		29VE010-250		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	200		250		ns
T_{CE}	Chip Enable Access Time		200		250	ns
T_{AA}	Address Access Time		200		250	ns
T_{OE}	Output Enable Access Time		100		120	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		50		50	ns
T_{OHZ}(1)	OE# High to High-Z Output		50		50	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

304 PGM T12.0

© 1998 Silicon Storage Technology, Inc.

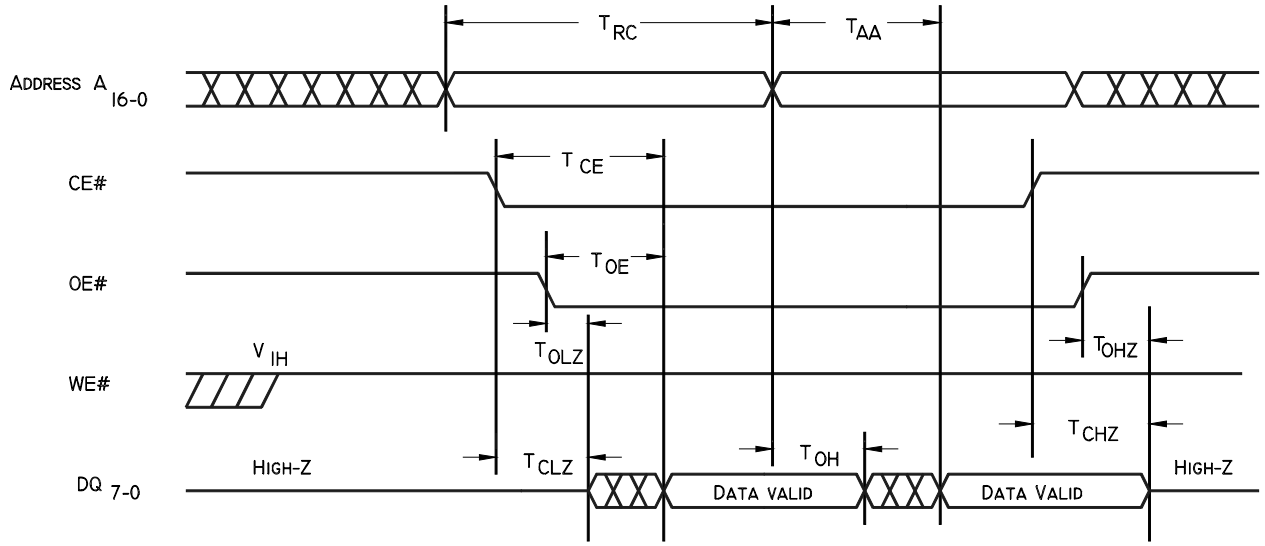
TABLE 13: PAGE-WRITE CYCLE TIMING PARAMETERS

		29EE010		29LE/VE010		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{WC}	Write Cycle (erase and program)		10		10	ms
T_{AS}	Address Setup Time	0		0		ns
T_{AH}	Address Hold Time	50		70		ns
T_{CS}	WE# and CE# Setup Time	0		0		ns
T_{CH}	WE# and CE# Hold Time	0		0		ns
T_{OES}	OE# High Setup Time	0		0		ns
T_{OEH}	OE# High Hold Time	0		0		ns
T_{CP}	CE# Pulse Width	70		120		ns
T_{WP}	WE# Pulse Width	70		120		ns
T_{DS}	Data Setup Time	35		50		ns
T_{DH}	Data Hold Time	0		0		ns
T_{BLC}(1)	Byte Load Cycle Time	0.05	100	0.05	100	µs
T_{BLCO}(1)	Byte Load Cycle Time	200		200		µs
T_{IDA}	Software ID Access and Exit Time		10		10	µs
T_{SCE}	Software Chip Erase		20		20	ms

304 PGM T13.1

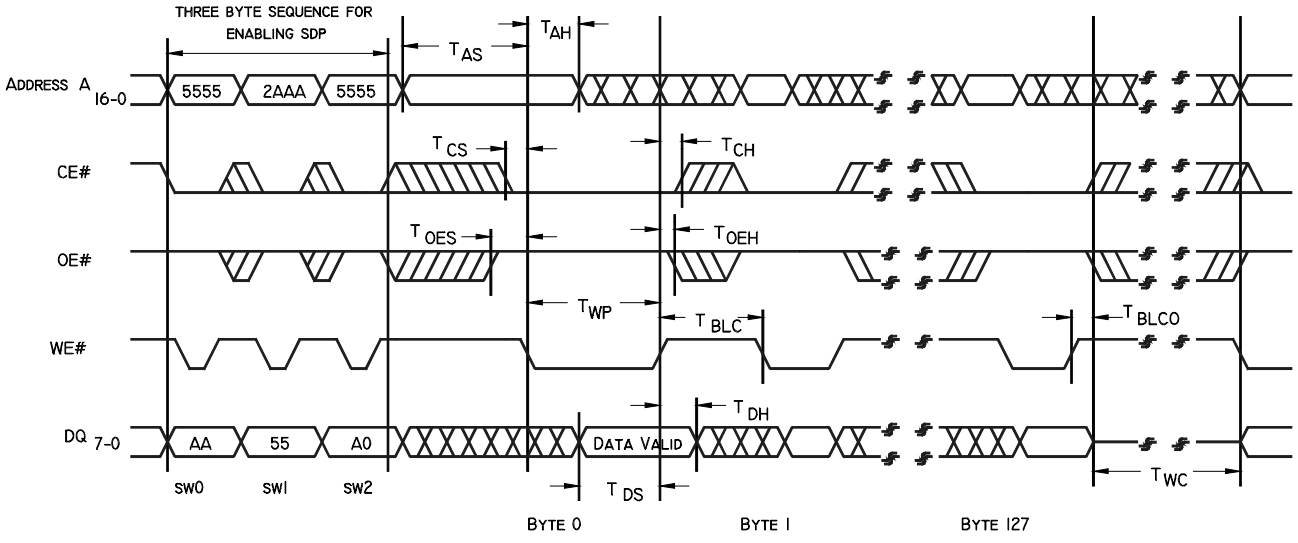
Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

© 1998 Silicon Storage Technology, Inc.



304 AC F03.0

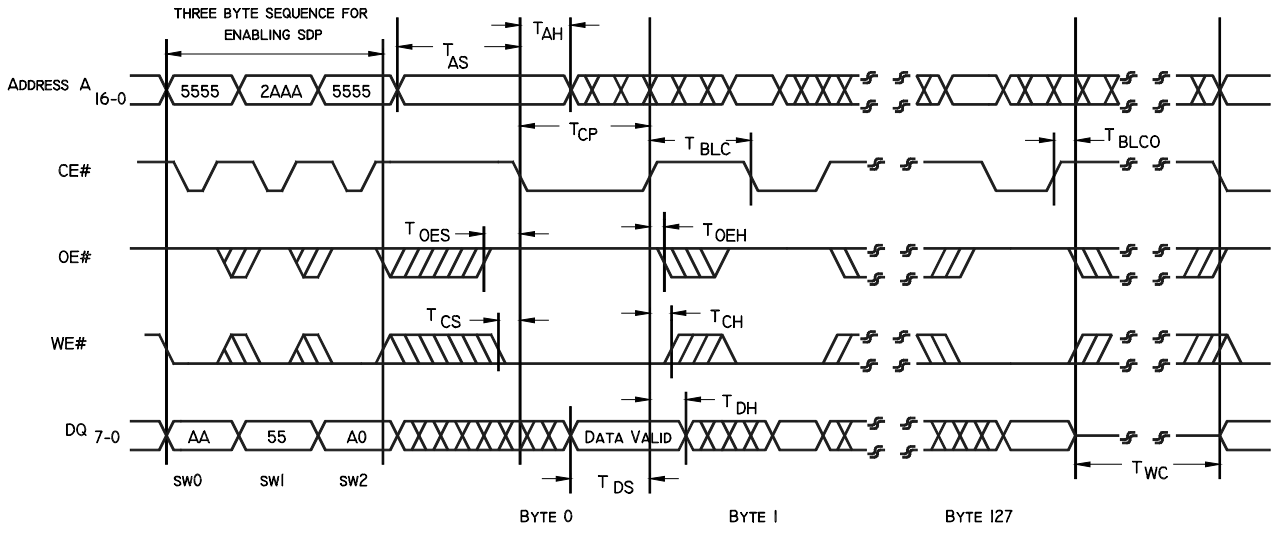
FIGURE 3: READ CYCLE TIMING DIAGRAM



304 AC F04.0

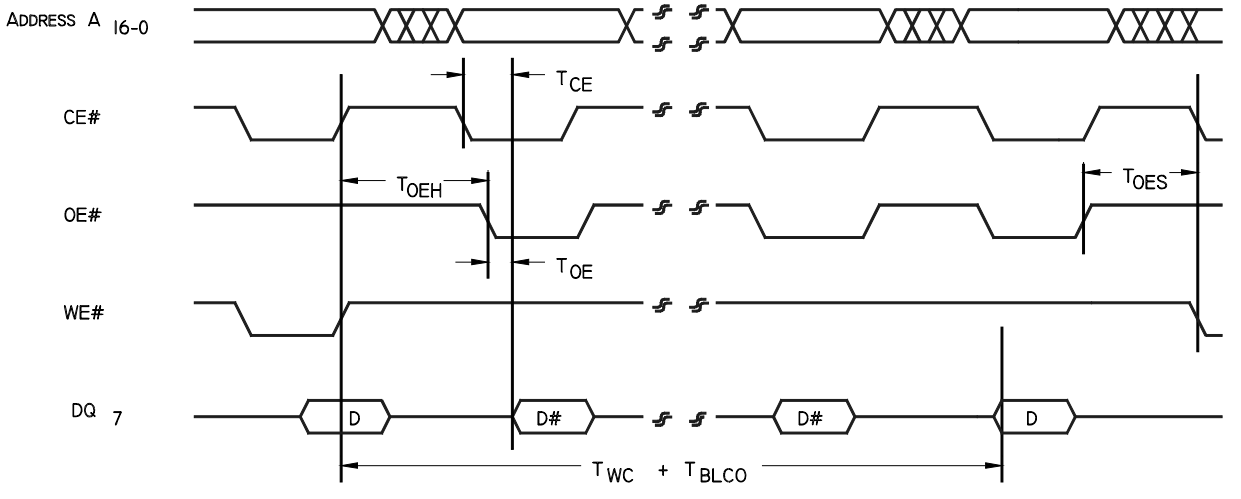
FIGURE 4: WE# CONTROLLED PAGE WRITE CYCLE TIMING DIAGRAM

© 1998 Silicon Storage Technology, Inc.



304 AC F05.0

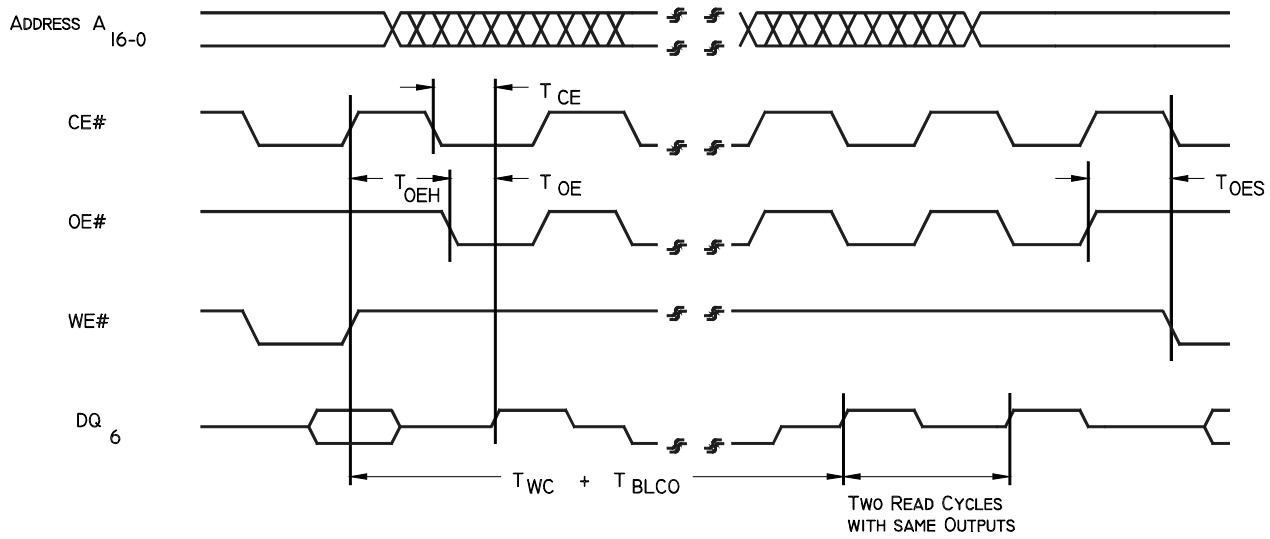
FIGURE 5: CE# CONTROLLED PAGE WRITE CYCLE TIMING DIAGRAM



304 AC F06.0

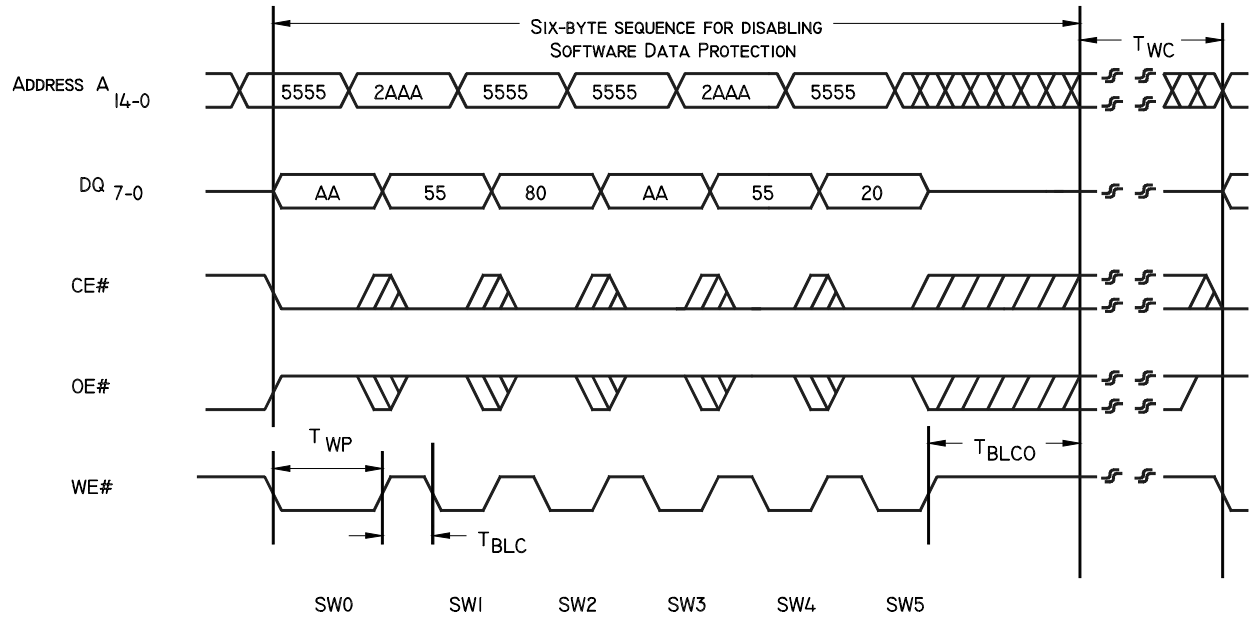
FIGURE 6: DATA# POLLING TIMING DIAGRAM

© 1998 Silicon Storage Technology, Inc.



304 AC F07.0

FIGURE 7: TOGGLE BIT TIMING DIAGRAM



304 AC F08.0

FIGURE 8: SOFTWARE DATA PROTECT DISABLE TIMING DIAGRAM

© 1998 Silicon Storage Technology, Inc.

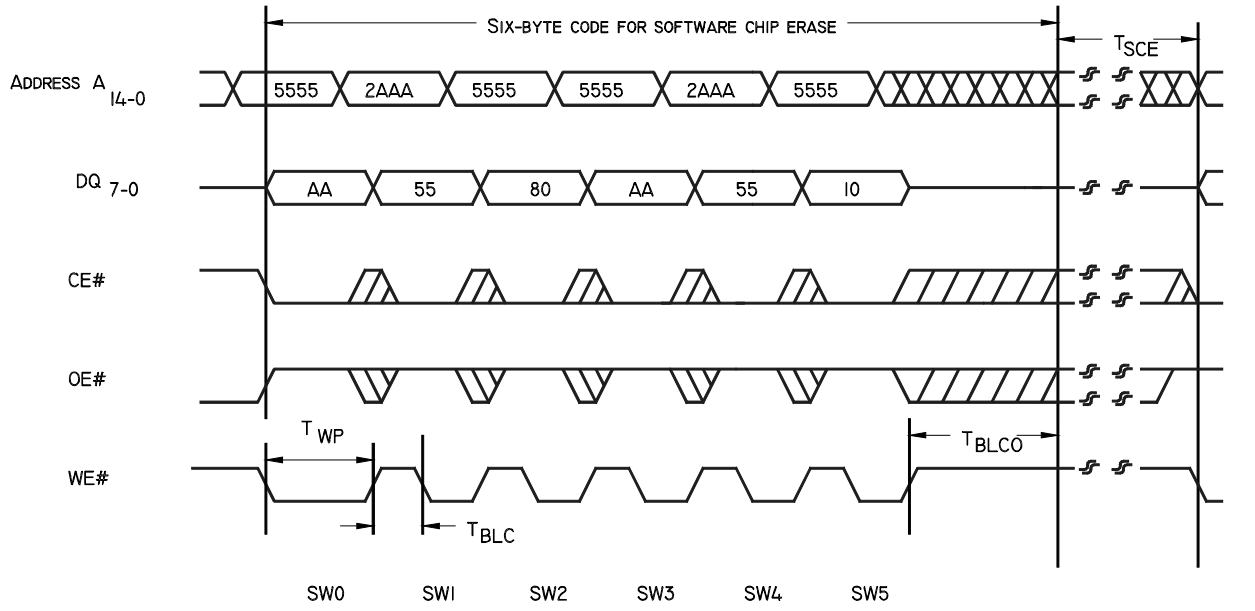


FIGURE 9: SOFTWARE CHIP ERASE TIMING DIAGRAM

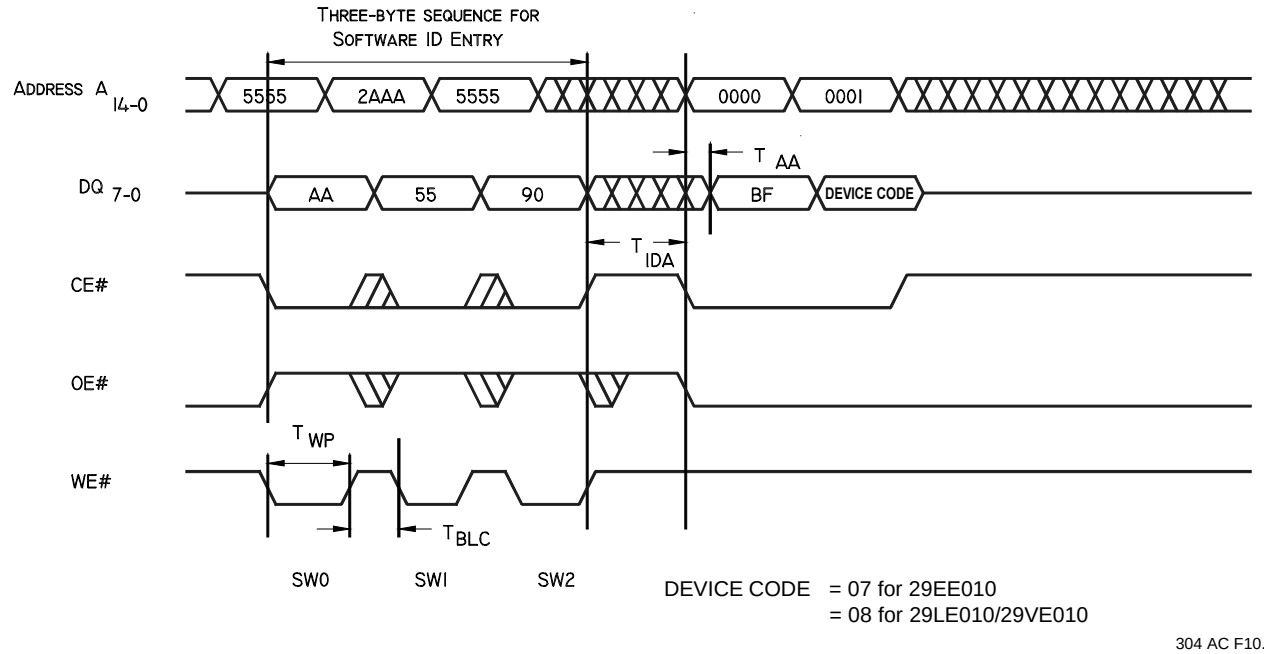


FIGURE 10: SOFTWARE ID ENTRY AND READ

© 1998 Silicon Storage Technology, Inc.

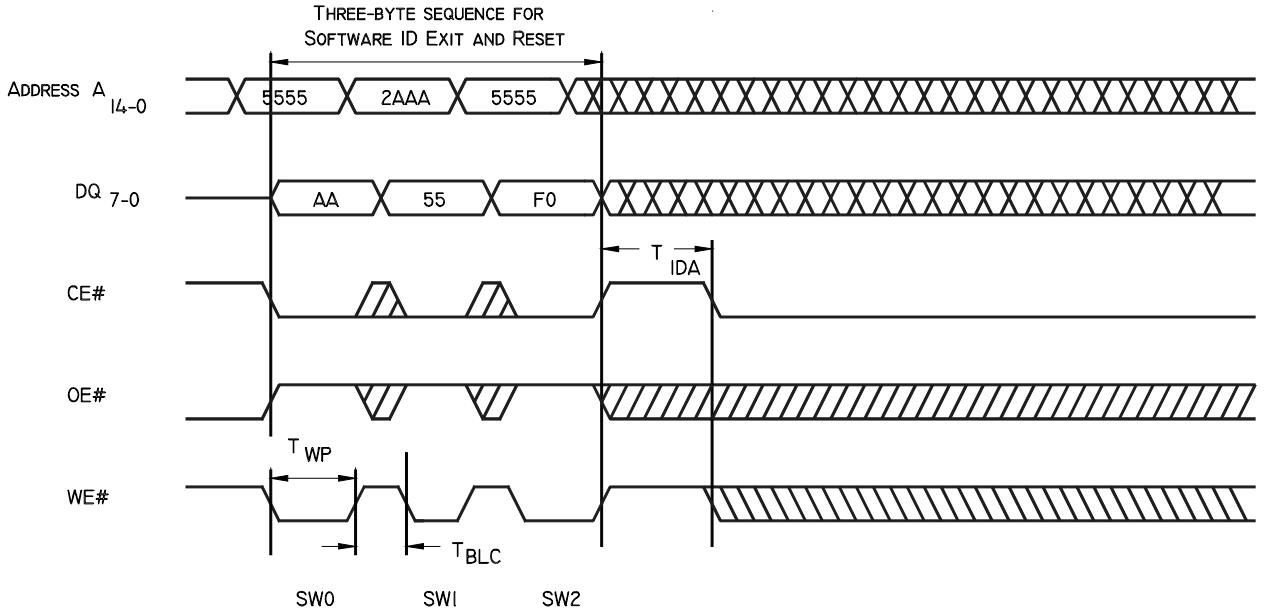
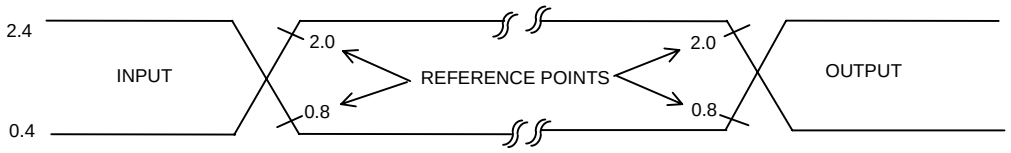


FIGURE 11: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

FIGURE 12: AC INPUT/OUTPUT REFERENCE WAVEFORMS

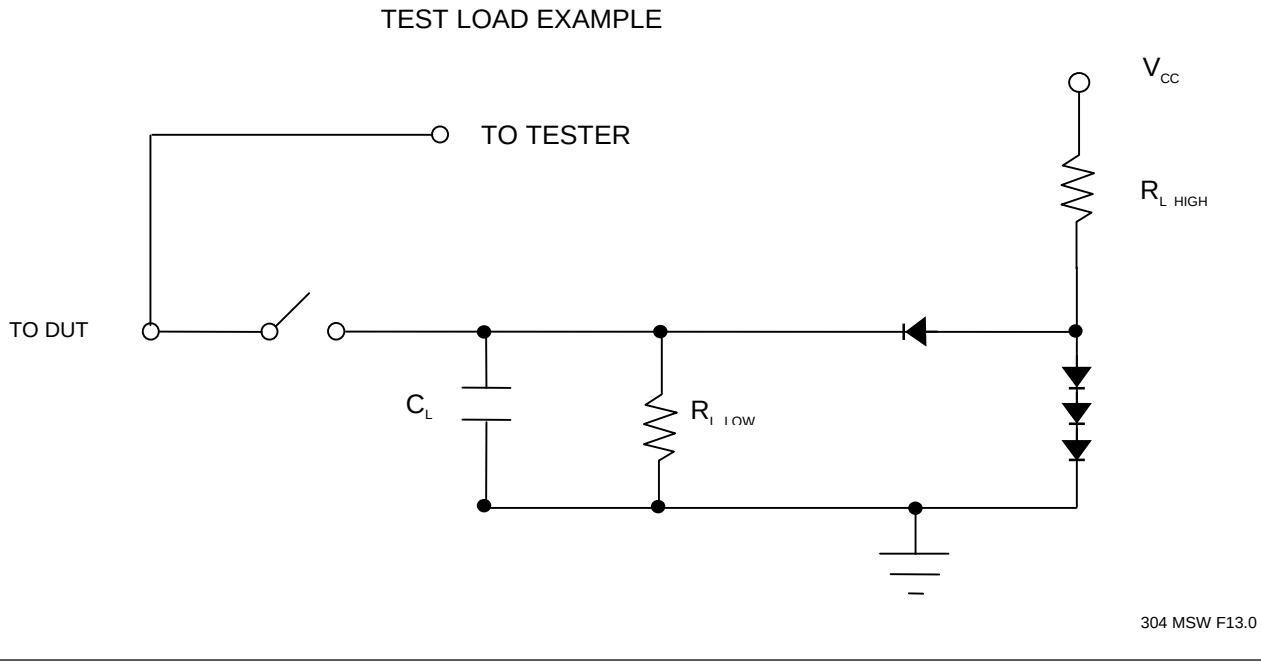


FIGURE 13: TEST LOAD EXAMPLE

© 1998 Silicon Storage Technology, Inc.

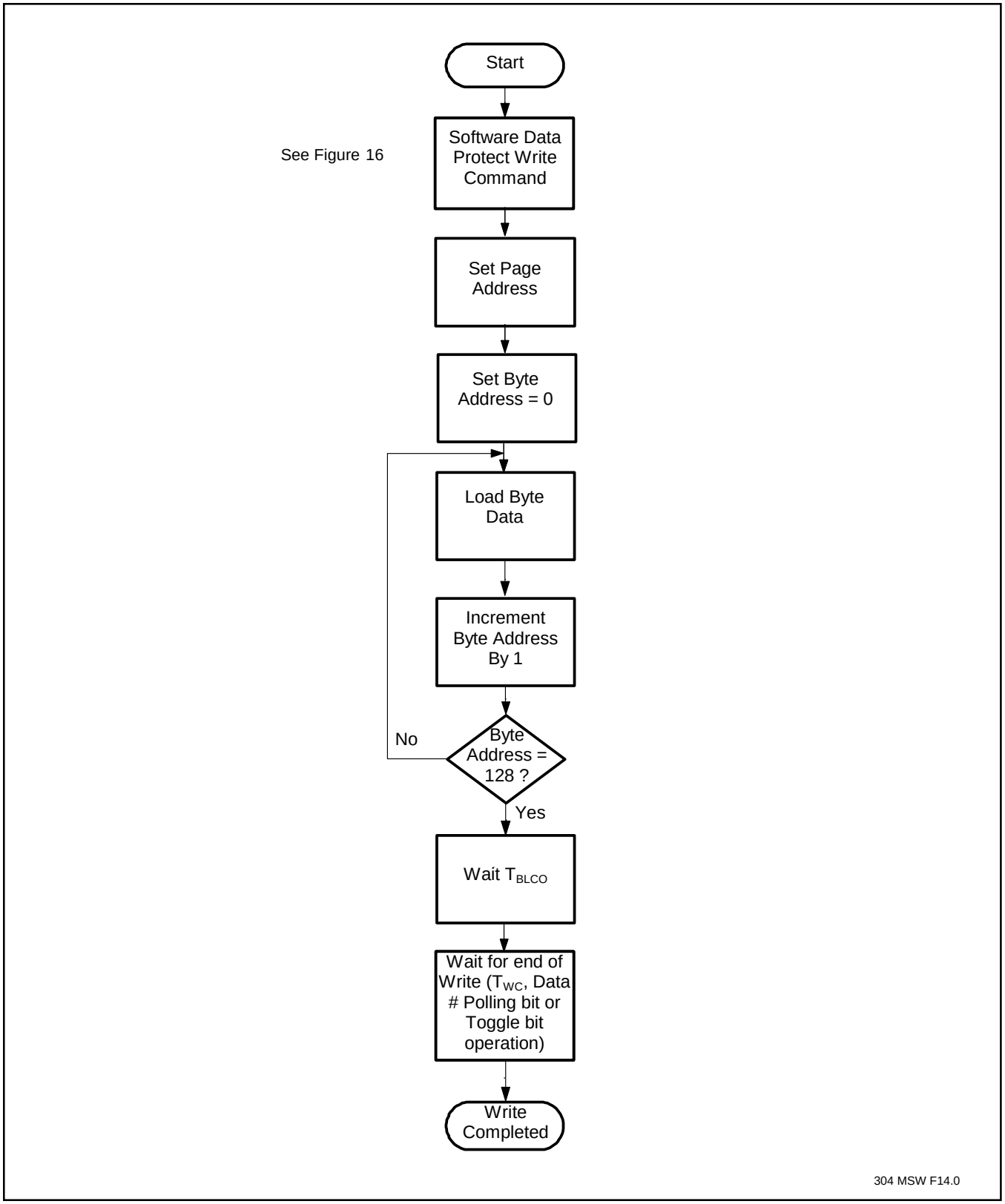


FIGURE 14: WRITE ALGORITHM

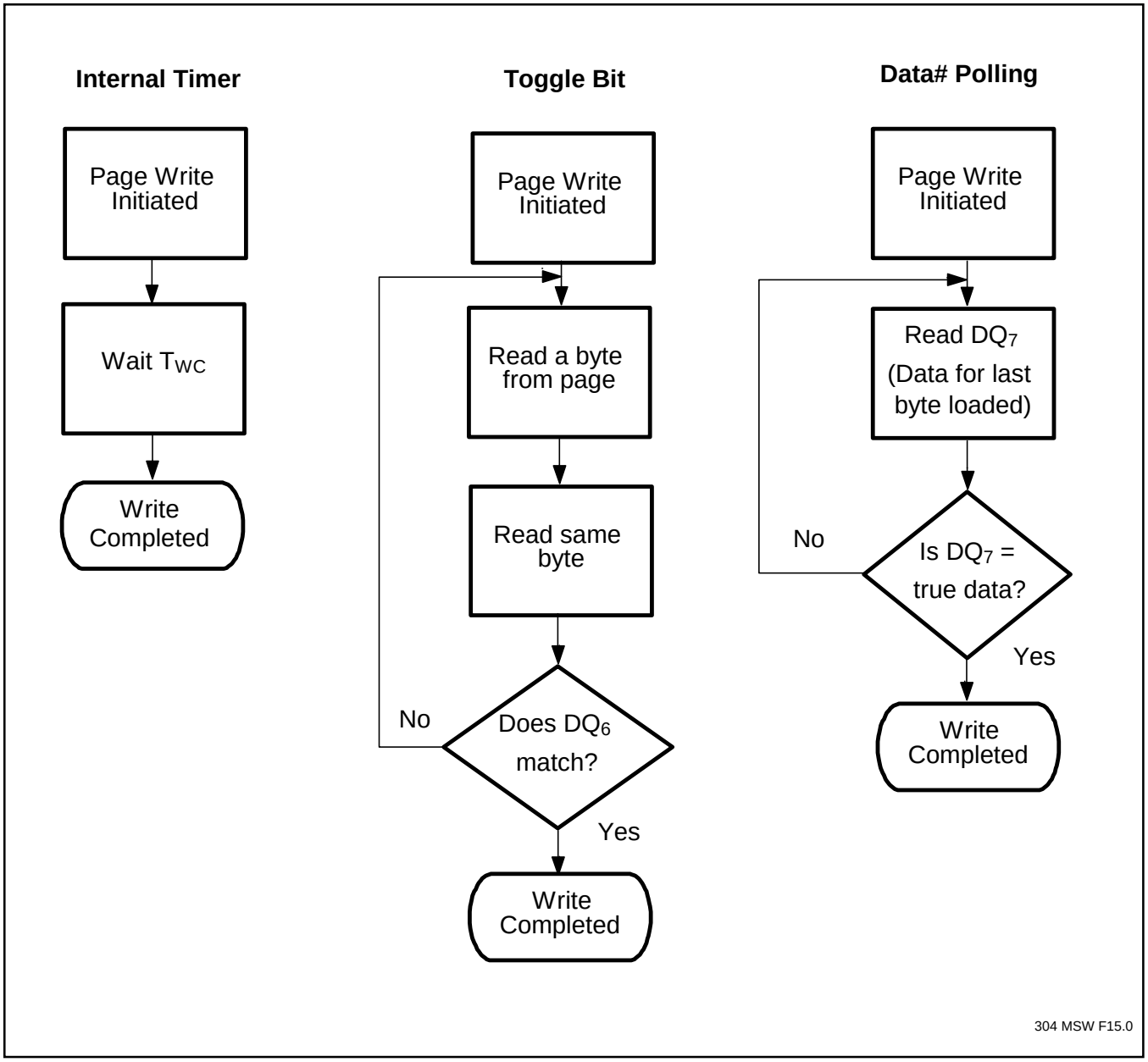


FIGURE 15: WAIT OPTIONS

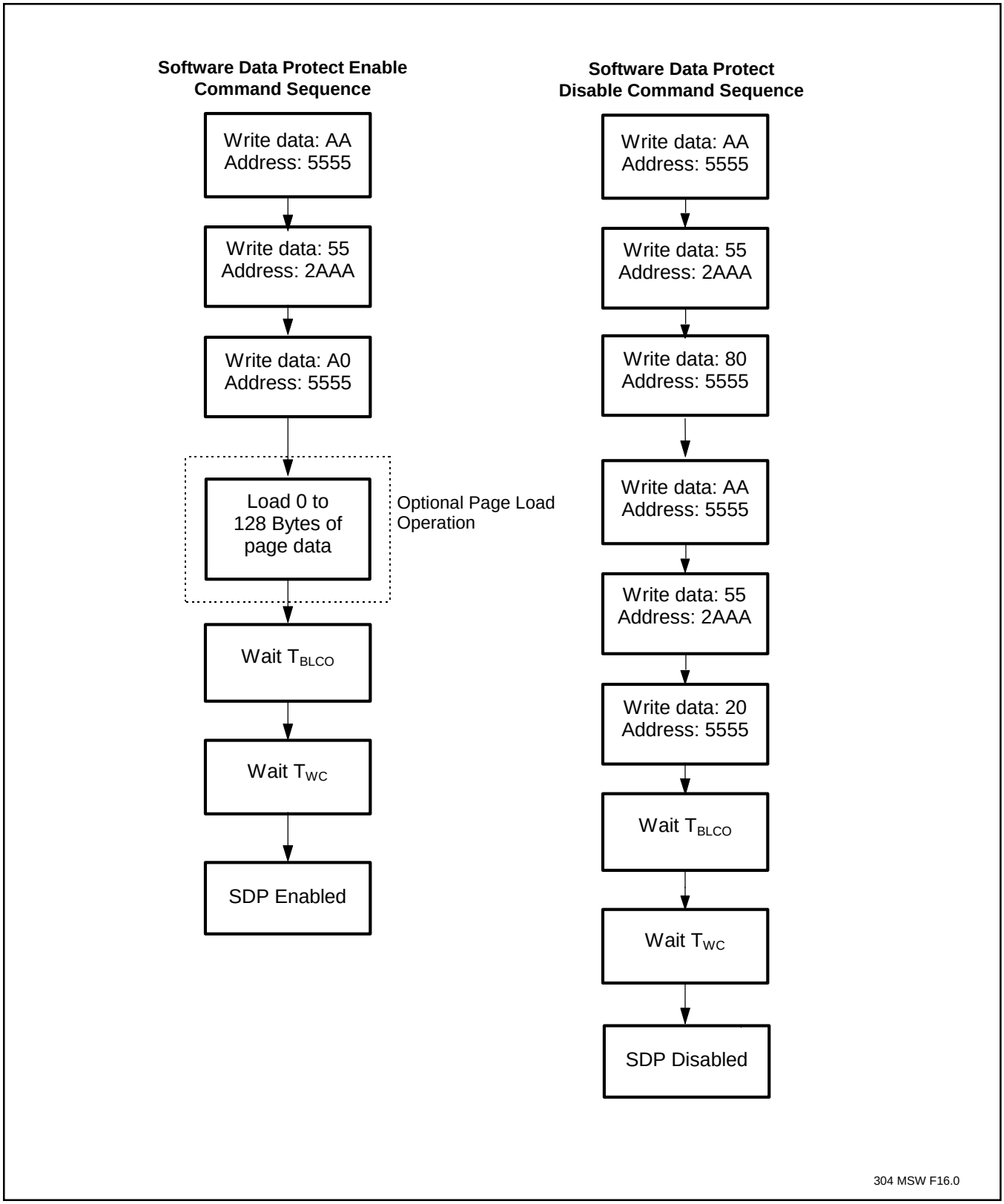

Software Data Protect Enable Command Sequence
Write data: AA Address: 5555
Write data: 55 Address: 2AAA
Write data: A0 Address: 5555
Load 0 to 128 Bytes of page data
Optional Page Load Operation
Wait T_{BLCO}
Wait T_{WC}
SDP Enabled
Software Data Protect Disable Command Sequence
Write data: AA Address: 5555
Write data: 55 Address: 2AAA
Write data: 80 Address: 5555
Write data: AA Address: 5555
Write data: 55 Address: 2AAA
Write data: 20 Address: 5555
Wait T_{BLCO}
Wait T_{WC}
SDP Disabled
304 MSW F16.0

FIGURE 16: SOFTWARE DATA PROTECTION FLOWCHARTS

© 1998 Silicon Storage Technology, Inc.

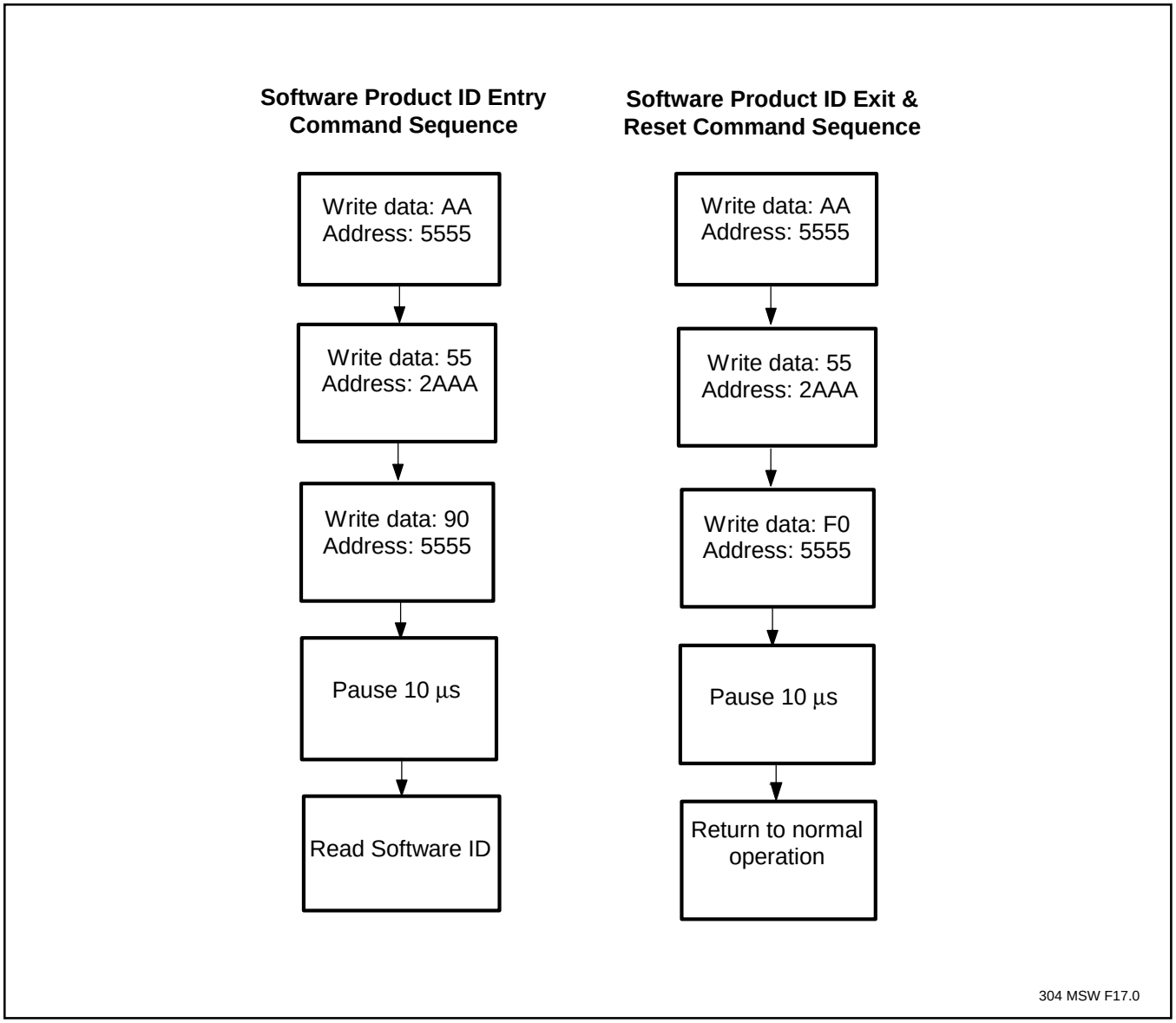


FIGURE 17: SOFTWARE PRODUCT COMMAND FLOWCHARTS

© 1998 Silicon Storage Technology, Inc.

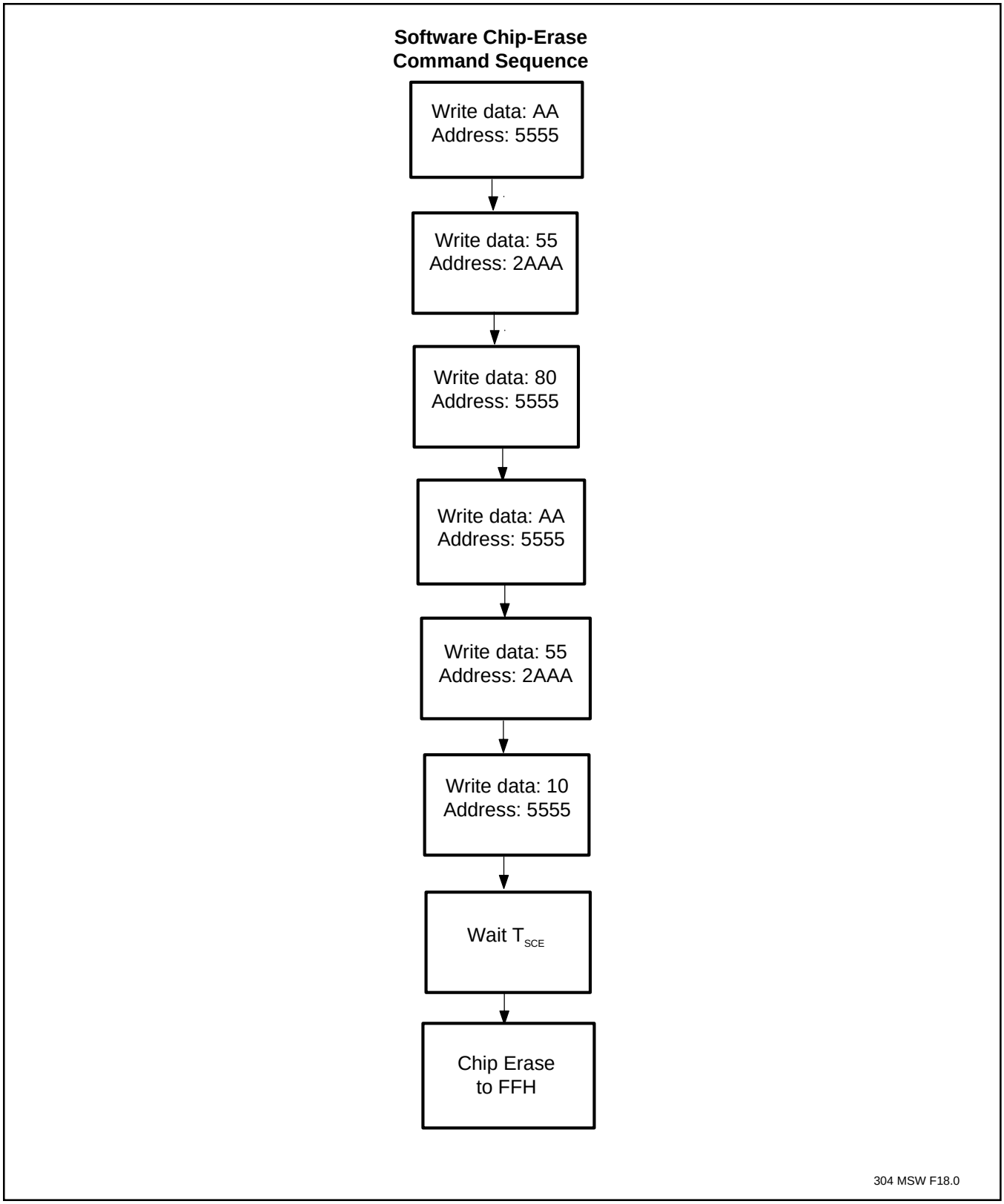


FIGURE 18: SOFTWARE CHIP ERASE COMMAND CODES

PRODUCT ORDERING INFORMATION

Device		Speed		Suffix1		Suffix2
SST29XE010	-	XXX	-	XX	-	XX

Package Modifier
- H = 32 leads
- Numeric = Die modifier

Package Type
- P = PDIP
- N = PLCC
- E = TSOP (die up) 8x20 mm
- W = TSOP (die up) 8x14 mm
- U = Unencapsulated die

Operating Temperature
- C = Commercial = 0° to 70°C
- I = Industrial = -40° to 85°C

Minimum Endurance
- 3 = 1000 cycles
- 4 = 10,000 cycles

Read Access Speed
- 250 = 250 ns
- 200 = 200 ns
- 150 = 150 ns
- 120 = 120 ns
- 90 = 90 ns

Voltage
- E = 5V-only
- L = 3V-only
- V = 2.7V-only

© 1998 Silicon Storage Technology, Inc.

29EE010 Valid combinations

SST29EE010- 90-4C- EH	SST29EE010- 90-4C- NH	SST29EE010- 90-4C- PH
SST29EE010-120-4C- EH	SST29EE010-120-4C- NH	SST29EE010-120-4C- PH
SST29EE010- 90-4C- WH		
SST29EE010-120-4C- WH		
SST29EE010- 90-4I-EH	SST29EE010- 90-4I-NH	
SST29EE010-120-4I-EH	SST29EE010-120-4I-NH	
SST29EE010-120-4C-U2		

29LE010 Valid combinations

SST29LE010-150-4C- EH	SST29LE010-150-4C- NH	SST29LE010-150-4C- PH
SST29LE010-200-4C- EH	SST29LE010-200-4C- NH	SST29LE010-200-4C- PH
SST29LE010-150-4C- WH		
SST29LE010-200-4C- WH		
SST29LE010-150-4I-EH	SST29LE010-150-4I-NH	
SST29LE010-200-4C-U2		

29VE010 Valid combinations

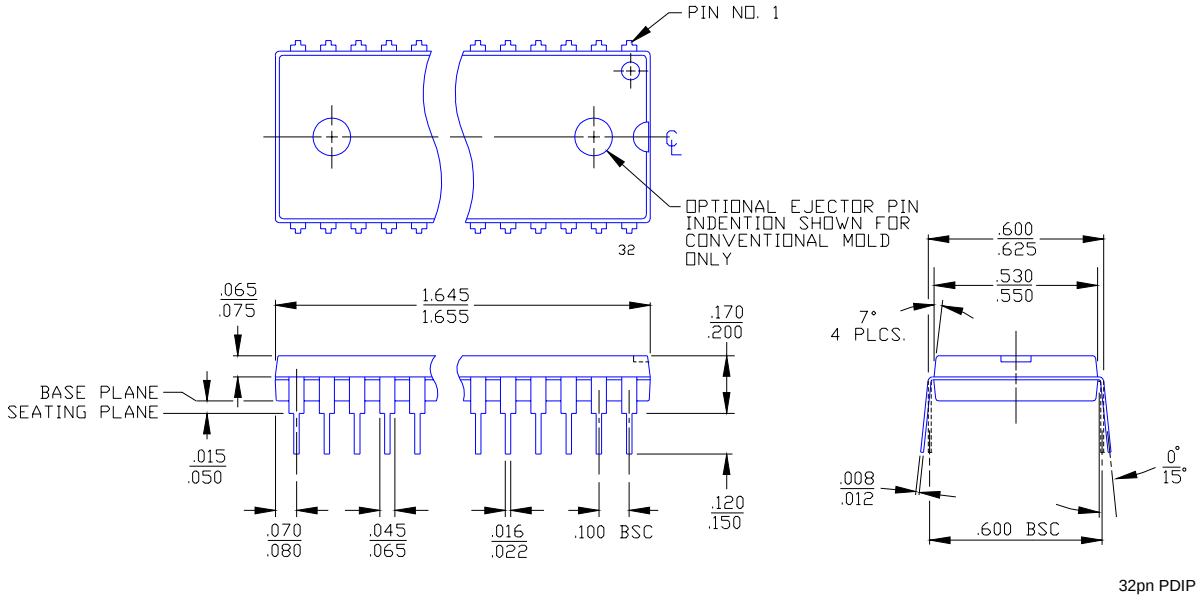
SST29VE010-200-4C- EH	SST29VE010-200-4C- NH	SST29VE010-200-4C- PH
SST29VE010-250-4C- EH	SST29VE010-250-4C- NH	SST29VE010-250-4C- PH
SST29VE010-200-4C-WH		
SST29VE010-250-4C-WH		
SST29VE010-200-4I-EH	SST29VE010-200-4I-NH	
SST29VE010-250-4C-U2		

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Note: The software chip erase function is not supported by the industrial temperature part. Please contact SST, if you require this function for an industrial temperature part.

© 1998 Silicon Storage Technology, Inc.

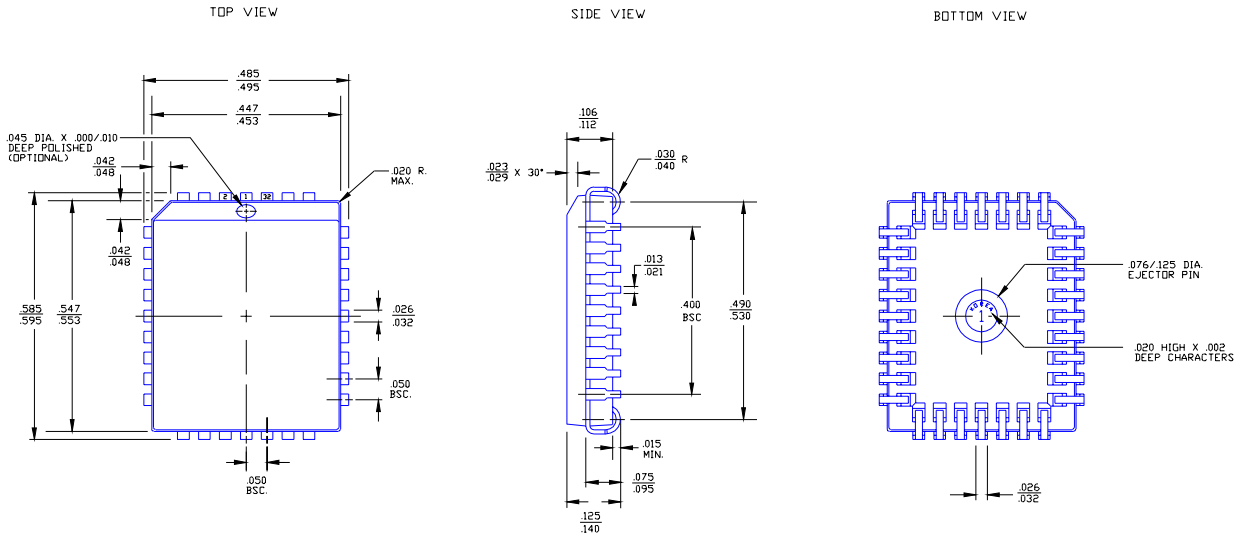
PACKAGING DIAGRAMS



32pn PDIP PH AC.2

Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH

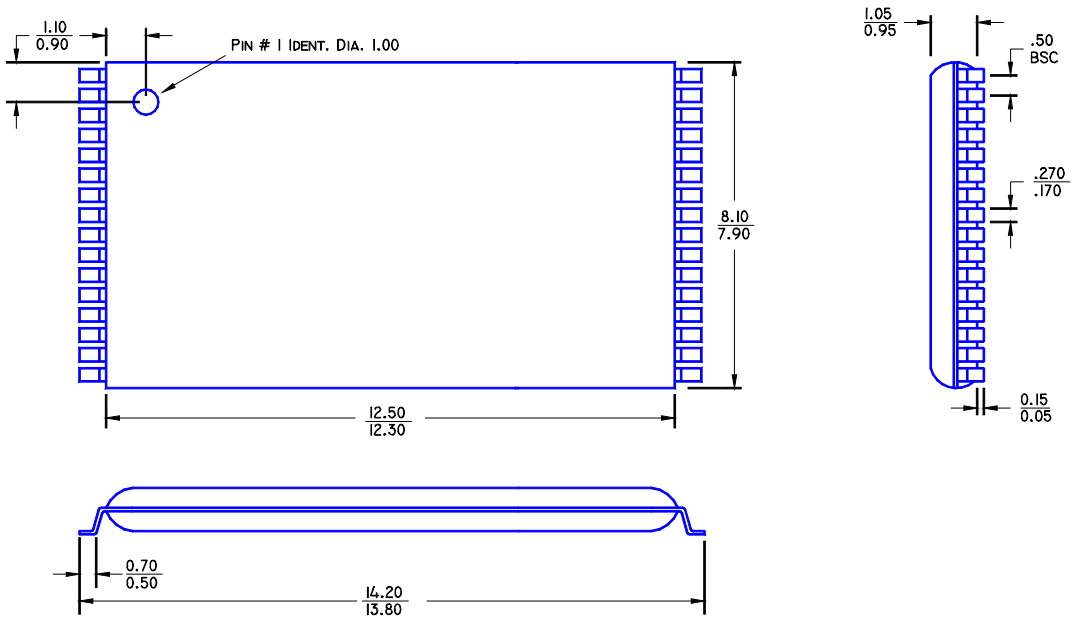


32pn PLCC NH AC.2

Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH

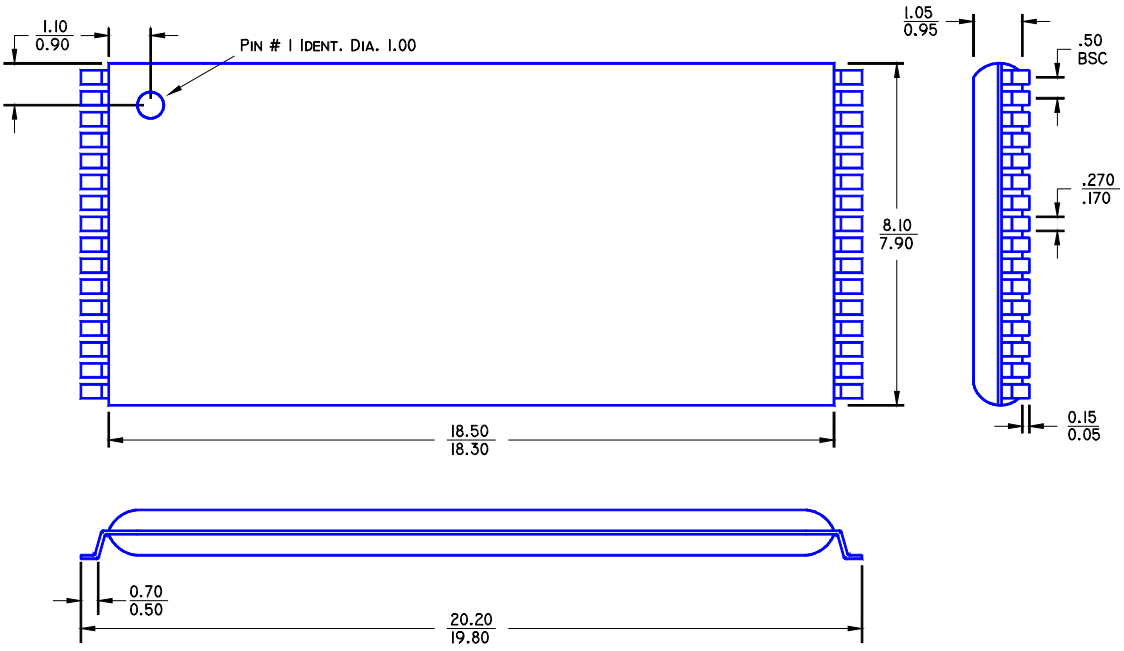
© 1998 Silicon Storage Technology, Inc.



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32pn TSOP WH AC.3

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: WH



Note: 1. Complies with JEDEC publication 95 MO-142 BD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32pn TSOP EH AC.4

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: EH

© 1998 Silicon Storage Technology, Inc.

SST Area Offices

U.S.A. - California	(408) 523-7722
U.S.A. - Florida	(813) 771-8819
U.S.A. - Florida	(941) 505-8893
U.S.A. - Massachusetts	(978) 356-3845
Japan - Yokohama	(81) 45-471-1851
Europe - UK	(44) 1784-490455

North American Sales Representatives

Alabama	
Elcom, Inc.	(205) 830-4001
Arizona	
QuadRep, Inc.	(602) 839-2102
California	
Northern	
Premier Technical Sales	(408) 736-2260
Southern	
QuadRep, Inc., San Diego	(619) 775-1188
QuadRep, Inc., Irvine	(714) 727-4222
Colorado	
QuadRep, Inc.	(303) 771-6886
Florida	
MEC Corporation - Central/East Coast	(904) 427-7236
MEC Corporation - South/East Coast	(954) 426-8944
MEC Corporation - West Coast	(813) 393-5011
Georgia	
Elcom, Inc.	(770) 447-8200
Iowa	
Oasis Sales Corporation	(319) 377-8738
Idaho	
QuadRep, Inc.	(208) 939-9626
Illinois	
Oasis Sales Corporation - Northern	(847) 640-1850
Rush & West Associates - Southern	(314) 965-3322
Kansas	
Rush & West Associates	(913) 764-2700
Massachusetts	
S-J Associates	(978) 670-8899
Minnesota	
Cahill, Schmitz & Cahill	(612) 646-7217
Missouri	
Rush & West Associates	(314) 965-3322
North Carolina	
Elcom, Inc. - Charlotte	(704) 543-1229
Elcom, Inc. - Raleigh	(919) 743-5200
New Jersey	
S-J Associates	(609) 866-1234
New Mexico	
QuadRep, Inc.	(505) 332-2417
New York	
S-J Associates - NYC	(516) 536-4242
S-J Associates - Upstate	(716) 924-1720
Ohio	
Great Lakes - Columbus	(614) 885-6700
Great Lakes - Cleveland	(216) 349-2700
Oregon	
Thorson Pacific, Inc.	(503) 293-9001
Texas	
Tech. Mktg, Inc. - Carrollton	(972) 387-3601
Tech. Mktg, Inc. - Houston	(713) 783-4497
Tech. Mktg, Inc. - Austin	(512) 343-6976
Utah	
QuadRep, Inc.	(801) 521-4717
Virginia	
S-J Associates	(703) 533-2233
Washington	
Thorson Pacific, Inc.	(425) 603-9393
Wisconsin	
Oasis Sales Corporation	(414) 782-6660
Canada - Toronto	
Kaltron Components Inc.	(905) 405-6276
Canada - Ottawa	
Kaltron Components Inc.	(819) 457-1225
Canada - Montreal	
Kaltron Components Inc.	(514) 696-6589
Canada - B.C.	
Thorson Pacific, Inc.	(604) 294-3999
Puerto Rico	
MEC/Caribe	(787) 746-9897

International Sales Representatives & Distributors

Australia	
ACD	(61) 3-762 7644
Belgium	
Memec Brussels	(32) 2778-9850
China	
Actron Technology Co., Ltd.	(86) 21-6482-8021
Denmark	
Berendsen Components A/S	(45) 39-57-71-10
Ireland	
Memec Ireland LTD	(353) 61 411842
Finland	
OXXO OY AB	(358) 9-5842 600
France	
RepDesign	(33) 1 46 23 7990
A2M	(33) 1 46 23 7900
Germany	
Endrich Bauelemente Vertriebs GMBH	(49) 7452-60070
Metronik GmbH	(49) 89-61108-0
Hong Kong	
Actron Technology Co., Ltd.	(852) 2727-3978
Serial System (HK) Ltd.	(852) 2950-0820
Israel	
Elina Electronics	(972) 3-649 8543
Italy	
Carla Gavazzi Cefra SpA	(39) 2-4801.2355
Japan	
Asahi Electronics Co., Ltd.	(81) 3-3350-5418
Asahi Electronics Co., Ltd.	(81) 93-511-6471
Hakuto Co., Ltd.	(81) 3-3355-7615
MICROTEK Inc.	(81) 3-5300-5525
Ryoden Trading Co., Ltd.	(81) 3-5396-6206
Silicon Technology Co., Ltd.	(81) 3-3795-6461
Korea	
Bigshine Korea Co., Ltd.	(82) 2-832-8881
Netherlands	
Memec Benelux	(31) 40-265-9399
Singapore	
Serial System Ltd.	(65) 286-1812
South Africa	
KH Distributors	(27) 11 845-5011
Spain	
Tekelec Espana S.A.	(34) 13 20 41 60
Sweden	
Pelcon Electronics AB	(46) 8.795 98 70
Switzerland	
Leading Technology	(41) 277-21 7-446
Taiwan, R.O.C.	
Award Software	(886) 22-555-0880
PCT Limited	(886) 22-698-0098
Tonsam Corporation	(886) 22-651-0011
United Kingdom	
Ambar Components, Ltd.	(44) 1844-261144

Revised 3-12-98